WHAT IS CLAIMED IS:

1. A bipolar transistor, comprising:

a substrate;

a semiconductor intrinsic base layer formed by blanket epitaxy on the substrate;

a collector layer formed on the substrate;

an emitter formed over the semiconductor intrinsic base layer, forming a junction between the semiconductor intrinsic base layer and the emitter, wherein the junction at a lateral portion of the emitter extends farther into the intrinsic base layer than the junction at a center portion of the emitter;

an extrinsic base formed adjacent to the lateral portion of the emitter;

a base electrode formed on a portion of the extrinsic base layer;

a collector electrode formed on a portion of the collector layer; and

an emitter electrode formed on a portion of the emitter layer.

2. A bipolar transistor as claimed in claim 1, wherein the emitter comprises a pedestal having a top which contacts an emitter layer.

3. A bipolar transistor as recited in claim 1, wherein a raised extrinsic base layer is formed and comprises one of a highly-doped polysilicon or a highly-doped amorphous

silicon.

4. A transistor as recited in claim 1, wherein the lateral portion has a depth in a range of approximately 20-40 nm.

5. A bipolar transistor as recited in claim 1, wherein the semiconductor intrinsic base layer comprises silicon germanium.

6. A bipolar transistor as recited in claim 1, further comprising a sidewall spacer formed between and electrically isolating the emitter and the extrinsic base layer.

7. A bipolar transistor as recited in claim 6, wherein the sidewall spacer comprises one of a silicon nitride, a silicon dioxide, or a combination of the two.

8. A bipolar transistor as recited in claim 7, wherein the sidewall spacer has a width in the range of 10 to 70 nanometers.

9. A bipolar transistor as recited in claim 2, wherein the emitter comprises one of a polysilicon or an amorphous silicon.

10. A bipolar transistor as recited in claim 1, wherein the emitter layer has a thickness in the range of 30 to 200 nanometers.

11. A bipolar transistor as recited in claim 1, wherein the emitter is in-situ doped with phosphorous that minimizes drive-in and activation anneal temperatures.

12. A method of making a bipolar transistor, comprising:

providing a semiconductor intrinsic base layer on a substrate;

providing a collector layer on the substrate;

providing a semiconductor intrinsic base layer on the substrate;

providing a mandrel or removable region in the location of an emitter;

providing a recess adjacent to mandrel films into the semiconductor intrinsic base layer to form a silicon pedestal;

providing an insulating spacer adjacent to the silicon pedestal and mandrel films;

providing an emitter on the semiconductor intrinsic base layer which contacts the intrinsic base layer in the former location of the mandrel films and which extends a distance wider than the silicon pedestal and a distance below a top surface of the silicon pedestal, the semiconductor intrinsic base layer forming a junction with the emitter;

providing a base electrode on a portion of raised extrinsic base layer;

providing a collector electrode on a portion of the collector layer; and

providing an emitter electrode on a portion of the emitter layer.

13. A method of making a bipolar transistor as recited in claim 13, wherein the

recess has a thickness in the range of 5 to 50 nanometers.

14. A method of making a bipolar transistor as recited in claim 13, wherein a raised extrinsic base layer is formed and comprises one of a highly-doped polysilicon or a highly-doped amorphous silicon.

15. A method of making a bipolar transistor as recited in claim 13, wherein the bipolar transistor is a heterojunction bipolar transistor.

16. A method of making a bipolar transistor as recited in claim 13, wherein the semiconductor intrinsic base layer comprises silicon germanium.

17. A method of making a bipolar transistor as recited in claim 13, wherein a sidewall spacer formed between and electrically isolating the emitter layer and the extrinsic base layer.

18. A method of making a bipolar transistor as recited in claim 17, wherein one of a silicon nitride, a silicon dioxide, or a combination of the two is used for the sidewall spacer.

19. A method of making a heterojunction bipolar transistor as recited in claim 17, wherein the sidewall spacer is provided with a width in the range of 10 to 70 nanometers.

20. A method of making a heterojunction bipolar transistor as recited in claim 13, wherein one of a polysilicon or an amorphous silicon is used for the emitter layer.

21. A method of making a heterojunction bipolar transistor as recited in claim 13, wherein the emitter layer is provided with a thickness in the range of 30 to 200 nanometers.

22. A method of making a heterojunction bipolar transistor as recited in claim 13, further comprising in-situ doping the emitter layer with phosphorous to minimize drive-in and activation anneal temperatures.